

METHOD AND APPARATUS FOR DETERMINING
PARASITIC CAPACITANCES IN AN INTEGRATED CIRCUIT

ABSTRACT OF THE DISCLOSURE

5 A method of determining a capacitance for use in a
circuit simulation is provided. The method may include
determining a test structure capacitance of a test
structure, simulating a design structure, extracting a
design structure capacitance of the simulated design
10 structure, and calculating a parasitic capacitance of the
design structure. Calculating the parasitic capacitance
may comprise deducting the test structure capacitance
from the design structure capacitance.